PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Serial No.: 09/697,305 Confirmation No.: 4222

In re Application of:

Takaki YOSHIDA et al. Group Art Unit: 2133

Filed: October 27, 2000 Examiner: Joseph D. Torres

For: FAULT DETECTING METHOD AND LAYOUT METHOD FOR SEMICONDUCTOR INTEGRATED CIRCUIT

AMENDMENT

MAIL STOP RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

Before further examination of the above-identified continued application, please amend the claims as examined in the Final Office Action mailed November 29, 2004, as follows: